

**VERSA 1000: 8-Bit, 40 MHz, 64K, 1K RAM Embedded,
ISP FLASH, MCU**

Datasheet Rev 0.1

Preliminary

Overview

The VRS1000-40 is an 8051 based 8-bit single chip microcontroller that includes 64K bytes of In-System Programmable (ISP) Flash and 1K bytes of SRAM.

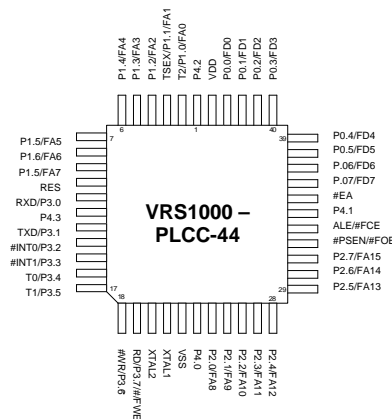
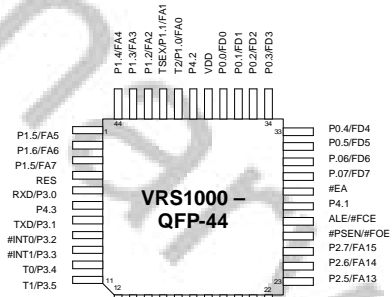
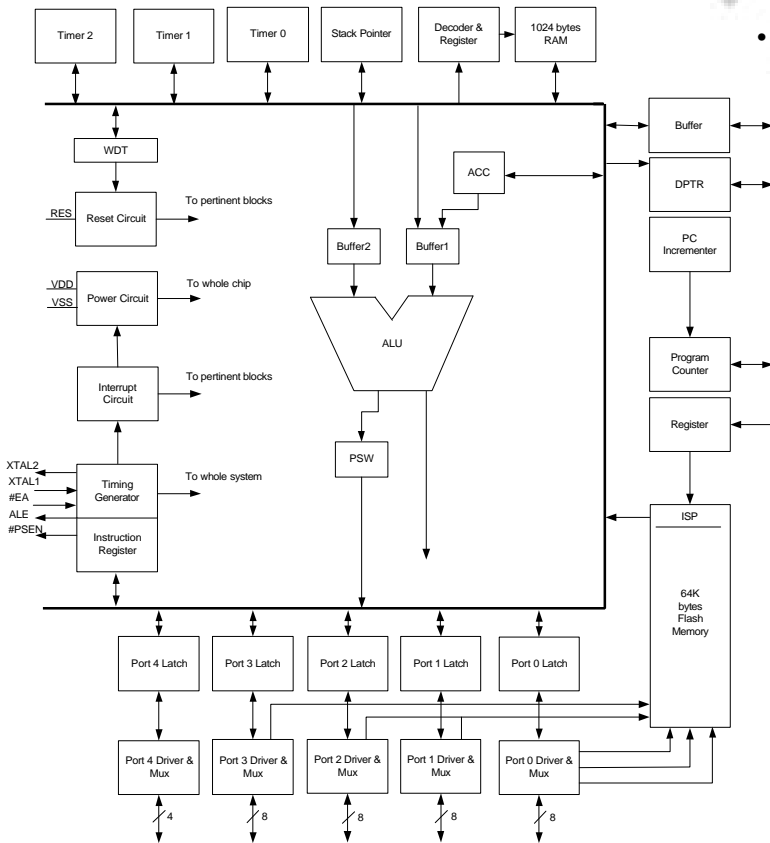
With its hardware features and powerful instruction set, the VRS1000-40 can be used as a versatile and cost effective microcontroller for applications that demand up to 36 I/Os or that require up to 64K bytes of Flash for either program and/or data memory.

The on-chip Flash memory can be programmed via a serial interface using the ISP feature. A commercial writer is available.

The VRS1000-40 is available in a 44-pin PLCC or QFP package.

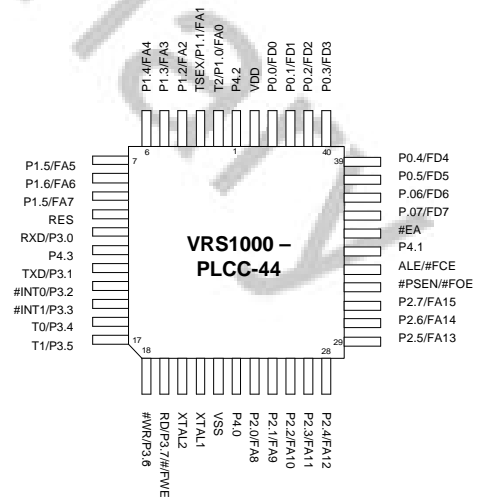
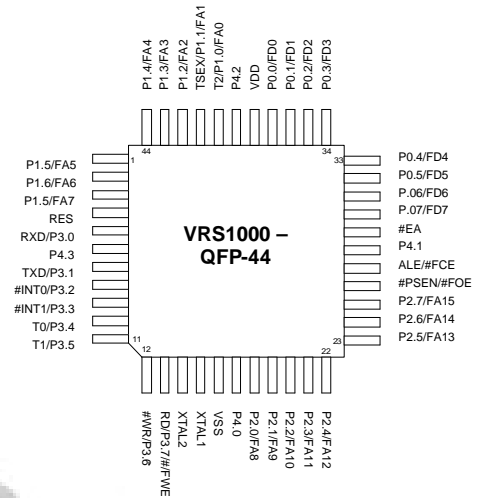
Features

- Operating voltage: 4.5V through 5.5V
- Program voltage: 5V
- General 80C52 family compatible
- 12 clocks per machine cycle
- 64K byte on-chip Flash memory with In-System Programming (ISP) capability
- 1024 byte on chip data RAM
- Three 16-bit Timers/Counters
- 1 Watch Dog Timer
- Four 8-bit I/Os + one 4-bit I/O
- Full duplex serial port
- Bit operation instruction
- Page free jumps
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply BCD arithmetic
- Direct and Indirect Addressing
- Nested Interrupts
- 2 Priority level interrupts
- 1 Serial I/O port
- Power save modes:
 - Idle mode and power down mode
- Code protection function
- Low EMI (inhibit ALE)
- Reset with address \$00 blank initiates ISP service program
- ISP service program space configurable in N*512byte (N=0 to 8) size
- 5-Channel Specific PWM (SPWM)



Pin Descriptions for QFP-44/PLCC-44

QFP - 44	PLCC - 44	Name	Active	I/O	Function
40	2	T2/P1.0		I/O	Timer 2 clock out & bit 0 of port 1
41	3	T2EX/P1.1		I/O	Timer 2 control & bit 1 of port 1
42	4	P1.2		I/O	Bit 2 of port 1
43	5	SPWM0/P1.3		I/O	SPWM Channel 0, bit 3 of port 1
44	6	SPWM1/P1.4		I/O	SPWM Channel 1, bit 4 of port 1
1	7	SPWM2/P1.5		I/O	SPWM Channel 2, bit 5 of port 1
2	8	SPWM3/P1.6		I/O	SPWM Channel 3, bit 6 of port 1
3	9	SPWM4/P1.7		I/O	SPWM Channel 4, bit 7 of port 1
4	10	RES	H	I	Reset
5	11	RXD/P3.0		I/O	Receive data & bit 0 of port 3
6	12	P4.3		I/O	Bit 3 of port 4
7	13	TXD/P3.1		I/O	Transmit data & bit 1 of port 3
8	14	#INT0/P3.2	L/ -	I/O	Low true interrupt 0 & bit 2 of port 3
9	15	#INT1/P3.3	L/ -	I/O	Low true interrupt 1 & bit 3 of port 3
10	16	T0/P3.4		I/O	Timer 0 & bit 4 of port 3
11	17	T1/P3.5		I/O	Timer 1 & bit 5 of port 3
12	18	#WR/P3.6	L/ -	I/O	Ext. memory write & bit 6 of port 3
13	19	#RD/P3.7	L/ -	I/O	Ext. memory read & bit 7 of port 3
14	20	XTAL2		O	Crystal out
15	21	XTAL1		I	Crystal in
16	22	VSS			Ground
17	23	P4.0		I	Bit 0 of port 4
18	24	P2.0/A8		I/O	Bit 0 of port 2 & bit 8 of external memory address
19	25	P2.1/A9		I/O	Bit 1 of port 2 & bit 9 of external memory address
20	26	P2.2/A10		I/O	Bit 2 of port 2 & bit 10 of external memory address
21	27	P2.3/A11		I/O	Bit 3 of port 2 & bit 11 of external memory address
22	28	P2.4/A12		I/O	Bit 4 of port 2 & bit 12 of external memory address
23	29	P2.5/A13		I/O	Bit 5 of port 2 & bit 13 of external memory address
24	30	P2.6/A14		I/O	Bit 6 of port 2 & bit 14 of external memory address
25	31	P2.7/A15		I/O	Bit 7 of port 2 & bit 15 of external memory address
26	32	#PSEN	L	O	Program storage enable
27	33	ALE	-	O	Address latch enable
28	34	P4.1		I	Bit 1 of Port 4
29	35	#EA	L	I	External access
30	36	PO.7/AD7			Bit 7 of port 0 & data/address bit 7 of external memory
31	37	PO.6/AD6		I/O	Bit 6 of port 0 & data/address bit 6 of external memory
32	38	PO.5/AD5		I/O	Bit 5 of port 0 & data/address bit 5 of external memory
33	39	PO.4/AD4		I/O	Bit 4 of port 0 & data/address bit 4 of external memory
34	40	PO.3/AD3		I/O	Bit 3 of port 0 & data/address bit 3 of external memory
35	41	PO.2/AD2		I/O	Bit 2 of port 0 & data/address bit 2 of external memory
36	42	PO. 1/AD1		I/O	Bit 1 of port 0 & data/address bit 1 of external memory
37	43	P0.0/AD0		I/O	Bit 0 of port 0 & data/address bit 0 of external memory
38	44	VDD			VCC
39	1	P4.2		I/O	Bit 2 of Port 4



Special Function Register (SFR)

Addresses \$80 to \$FF of the SFR address space can be accessed in direct addressing mode only. The following table lists the SFRs that are standard for 80C52 as well as VRS1000 extension SFRs.

\$F8											\$FF
\$F0	B				ISPFAH	ISPFAL	ISPFD	ISPC			\$F7
\$E8											\$EF
\$E0	ACC										\$E7
\$D8	P4										\$DF
\$D0	PSW										\$D7
\$C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2					\$CF
\$C0											\$C7
\$B8	IP								SCONF		\$BF
\$B0	P3										\$B7
\$A8	IE				SPWMD4						\$AF
\$A0	P2			SPWMC	SPWMD0	SPWMD1	SPWMD2	SPWMD3			\$A7
\$98	SCON	SBUF	P1CON						WDTC		\$9F
\$90	P1										\$97
\$88	TCON	TMOD	TL0	TL1	TH0	TH1					\$8F
\$80	P0	SP	DPL	DPH		RCON	DBANK	PCON			\$87

Note: The SFRs that are in bold are the extension Special Function Registers for the VRS1000.

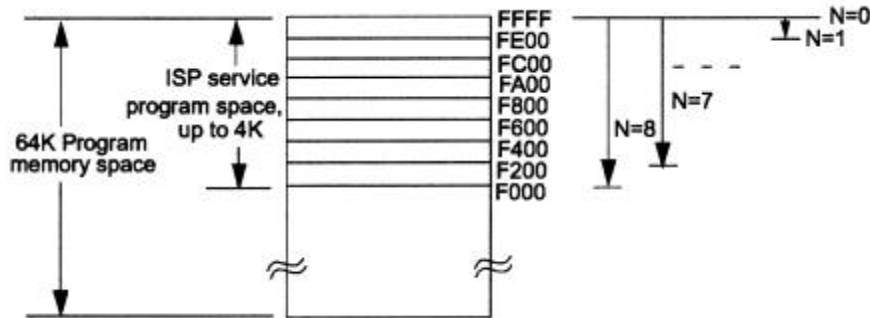
Addr	SFR	Reset	7	6	5	4	3	2	1	0
85H	RCON	*****00							RAMS1	RAMS0
86H	DBANK	0***0001	BS3				BSE	BS2	BS1	BS0
9BH	P1CON	0000***	SPWM4E	SPWM3E	SPWM2E	SPWM1E	SPWMOE			
9FH	WDTC	0*0**000	WDTE	CLEAR				PS2	PS1	PS0
A3H	SPWMC	*****00							FPDIV1	FPDIV0
A4H	SPWMD0	00H	SPWMD0.4	SPWMD0.3	SPWMD0.2	SPWMD0.1	SPWMD0.0	BRM0.2	BRM0.1	BRM0.0
A5H	SPWMD1	00H	SPWMD1.4	SPWMD1.3	SPWMD1.2	SPWMD1.1	SPWMD1.0	BRM1.2	BRM1.1	BRM1.0
A6H	SPWMD2	00H	SPWMD2.4	SPWMD2.3	SPWMD2.2	SPWMD2.1	SPWMD2.0	BRM2.2	BRM2.1	BRM2.0
A7H	SPWMD3	00H	SPWMD3.4	SPWMD3.3	SPWMD3.2	SPWMD3.1	SPWMD3.0	BRM3.2	BRM3.1	BRM3.0
ACH	SPWMD4	00H	SPWMD4.4	SPWMD4.3	SPWMD4.2	SPWMD4.1	SPWMD4.0	BRM4.2	BRM4.1	BRM4.0
BFH	SCONF	0***010	WDR					ISPE	OME	ALEI
D8H	P4	****1111					P4.3	P4.2	P4.1	P4.0
F4H	ISPFAH	00H	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
F5H	ISPFAL	00H	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
F6H	ISPFD	00H	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F7H	ISPC	0*****00	START						F1	F0

Description of Extension Function

Program Memory

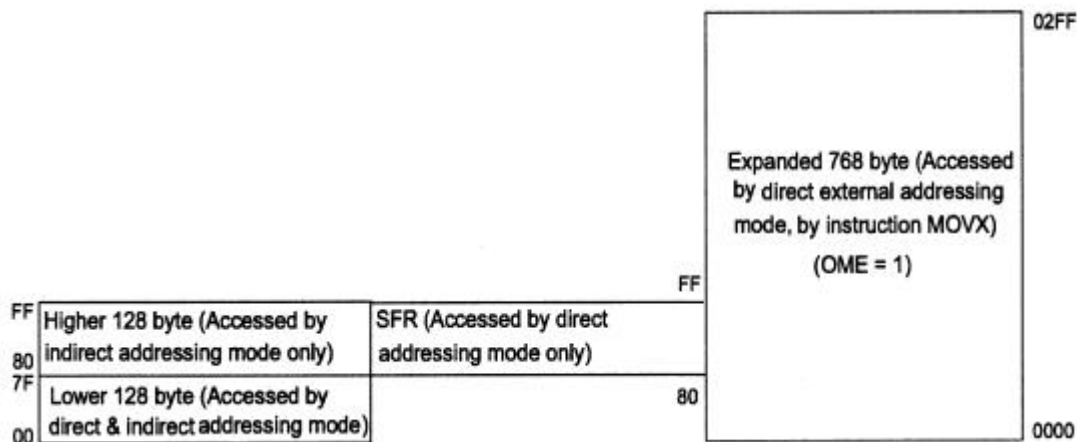
The VRS1000 includes 64K of on-chip Flash that can be used as general program memory. This memory space includes up to 4K bytes, which can be used for the ISP service program. The address range for the 64K Flash is \$0000 to \$FFFF and the address range for the ISP service program is \$F000 to \$FFFF.

The ISP service program size can be partitioned as N blocks of 512 bytes (where N=0 to 8). Setting N=0 corresponds to no ISP service program space available and the full 64K is configured as program memory. Setting N=1 reserves memory addresses \$FE00 to \$FFFF for the ISP service program and the remaining space for program memory. The value of N can be programmed into the VRS1000 by the user. The following figure describes the memory partitioning based on N.



Data Memory

The VRS1000 has 1K of on-chip SRAM. 256 bytes are configured as the standard 80C52 internal memory structure, while the remaining 768 bytes can be accessed by using external memory addressing (MOVX).



Data Memory - Lower 128 bytes (\$00 to \$7F, Bank 0 & Bank 1)

Data Memory \$00 to \$FF is the same as a standard 80C52.
The addresses \$00 to \$7F can be accessed by direct and indirect addressing modes.
Address range \$00 to \$1F is register area.
Address range \$20 to \$2F is memory bit area.
Address range \$30 to \$7F is for general memory area.

Data Memory - Higher 128 bytes (\$80 to \$FF, Bank 2 & Bank 3)

The addresses \$80 to \$FF can be accessed by indirect addressing or by bank mapping direct addressing mode.

Data Memory - Expanded 768 bytes (\$0000 to \$02FF, Bank 4 - Bank 15)

External addresses \$0000 to \$02FF is the on-chip expanded RAM area (768 bytes). This area can be accessed by external direct addressing (MOVX) or by bank mapping direct addressing. If the address of instruction MOVX @DPTR is larger than \$02FF, then the VRS1000 will generate the external memory control signal automatically.

Bit 1 (OME) of Special Function Register \$BF (SCONF) can enable or disable this expanded 768 bytes of SRAM. The default setting of OME bit is 1 (enabled). The address space of instruction MOVX @Ri, i=0,1 is determined by bit 1 & bit 0 (RAMS1, RAMS0) of special function register \$85 (RCON). The default setting of RAMS1, RAMS0 bits is 00 (page 0).

One page of data RAM is 256 bytes.

RAMS1, RAMS0=00, Rn of instruction MOVX @Ri, i=0,1 mapping to expanded RAM address \$0000 to \$00FF (page 0)
RAMS1

RAMS0=01, Rn of instruction MOVX @Ri, i=0,1 mapping to expanded RAM address \$0100 to \$01FF (page 1)

RAMS1, RAMS0=10, Rn of instruction MOVX @Ri, i=0,1 mapping to expanded RAM address \$0200 to \$02FF (page 2)

RAMS1, RAMS0=11, Rn of instruction MOVX @Ri, i=0,1 mapping to expanded RAM address \$XY00 to \$XYFF, whose high byte address is specified by port 2. (VRS1000 will generate the external memory control signals automatically).

Bank mapping direct addressing mode

SRAM bank address 40h-7Fh allows windowed access to all the 1K on-chip SRAM. This is described in the following table.

BS3	BS2	BS1	BS0	040h~07fh mapping address	Note
0	0	0	0	000h~03fh	lower 128 byte RAM
0	0	0	1	040h~07fh	lower 128 byte RAM
0	0	1	0	080h~0bfh	higher 128 byte RAM
0	0	1	1	0c0h~0ffh	higher 128 byte RAM
0	1	0	0	0000h~003fh	on-chip expanded 768 byte RAM
0	1	0	1	0040h~007fh	on-chip expanded 768 byte RAM
0	1	1	0	0080h~00bfh	on-chip expanded 768 byte RAM
0	1	1	1	00c0h~00ffh	on-chip expanded 768 byte RAM
1	0	0	0	0100h~013fh	on-chip expanded 768 byte RAM
1	0	0	1	0140h~017fh	on-chip expanded 768 byte RAM
1	0	1	0	0180h~01bfh	on-chip expanded 768 byte RAM
1	0	1	1	01c0h~01ffh	on-chip expanded 768 byte RAM
1	1	0	0	0200h~023fh	on-chip expanded 768 byte RAM
1	1	0	1	0240h~027fh	on-chip expanded 768 byte RAM
1	1	1	0	0280h~02bfh	on-chip expanded 768 byte RAM
1	1	1	1	02c0h~02ffh	on-chip expanded 768 byte RAM

With this bank-mapping scheme, the user can access the entire 1K bytes of on-chip SRAM using direct addressing.

Example, user writes #30h to \$101 address:

```
MOV  DBANK, #88H      ; set bank mapping $040-r$07f to $0100-$013f
MOV  A, #30H         ; store #30H to A
MOV  41H, A          ; write #30H to $0101 address
```

Data Bank Control Register (DBANK, \$86)

	bit-7				bit-0			
Read:	BSE	Unused	Unused	Unused	BS3	BS2	BS1	BS0
Write:								
Reset value:	0	*	*	*	0	0	0	1

Data bank select enable bit BSE = 1 enables the data bank select function
 Data bank select enable bit BSE = 0 disables the data bank select function
 BS[3:0] setting will map \$040-\$07F RAM space to entire 1K byte on-chip RAM space

Internal RAM Control Register (RCON, \$85)

	bit-7				bit-0			
Read:	Unused	Unused	Unused	Unused	Unused	Unused	RAMS1	RAMS0
Write:								
Reset value:	*	*	*	*	*	0	1	0

Note: "R" means reserved

The VRS1000 has 768 bytes of on-chip SRAM, which can be accessed by external memory addressing (MOVX). The address space of instruction MOVX @Rn is determined by bit 1 and bit 0 (RAMS1, RAMS0) of RCON. The default setting of RAMS1, RAMS0 bits is 00 (page 0).

System Control Register (SCONF, \$BF)

	bit-7				bit-0			
Read:	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Write:								
Reset value:	0	*	*	*	*	0	1	0

WDR: Watch Dog Timer Reset. When the system is reset by Watch Dog Timer overflow, WDR will be set to 1

ISPE: ISP function enable bit

OME: 768 byte on-chip RAM enable bit

ALEI: ALE output inhibit bit, to reduce EMI

Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.

The bit 1 (OME) of SCONF can enable or disable the on-chip expanded 768-byte RAM. The default setting of OME bit is 1 (enable).

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when the reset signal generated by WDT overflows.

Users should check WDR bit whenever an unpredicted reset happens.

Port 4

Port 4 has only 4 pins and its port address is located at OD8H. The function of port 4 is the same as the function of ports 1, 2 and 3.

Port 4 (P4, \$138)

	bit-7				bit-0			
Read:	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Write:	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Reset value:	0	*	*	*	1	1	1	1

Note: Bit 3, 2, 1, and 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively

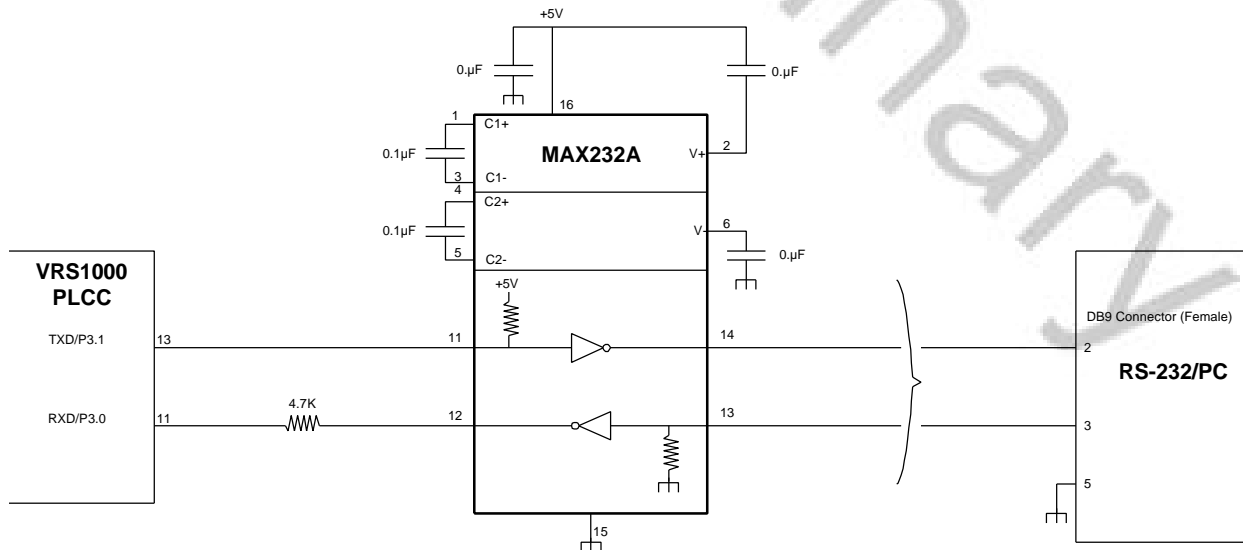
In-System Programming (ISP) Function

The VRS1000 is an ISP device and can, therefore, generate all internal control signals required for the Flash program, erase and protect functions. Any VRS1000 interface can be used to input this data onto the chip, provided that an ISP service program is loaded that can perform and control these functions. For example, if a user wishes to use the UART interface for ISP control by a host device, the ISP service program should include baud rate, checksum or parity check or any other error-checking mechanism to avoid data transmission error.

Note that the ISP service program can be initiated in VRS1000 active or idle mode. It cannot be initiated under power down mode.

The Figure below shows a typical connection for ISP.

Typical Connection Diagram



Lock Bit (N)

The Lock Bit N provides two functions: one is for service program size configuration. The other is for locking and, therefore, blocks the ISP service program space from accidental erasure.

The ISP service program space ranges from addresses \$F000 to \$FFFF. It can be partitioned into a block of N*512 byte (N=0 to 8). As previously mentioned, N=0 corresponds to no ISP function and all of the 64K byte Flash memory is configured as program memory. Setting N=1 sets the ISP service program size to 512 bytes and the remaining 63.5K bytes of Flash as program memory. The maximum ISP service program allowed is 4K bytes (N=8).

The ISP service program space is set downward from the top of the program address space (\$FFFF downwards). The start address of the ISP service program is located at \$Fx00 where x is an even number depending on the Lock Bit N. See Figure 4 for a diagram of the ISP service program space.

Note that the Lock Bit N function is not the same as the Flash protect function. The lock function serves to protect the locked ISP service program space from erasure. The Flash protect function, when activated, inhibits the entire Flash memory from being able to be read from the chip.

Run ISP Service Program

(1) Blank reset. Hardware reset with first flash address blank (\$0000=#FFH) will load the PC (program counter) with the start address of the ISP service program.

(2) Execute jump instruction program to PC.

User can initiate general 80C52 INT function to run the ISP service program. After the ISP service program is executed, the user must reset the VRS1000, either by a hardware reset or by a WDT, or jump to address \$0000 to re-start the firmware program.

ISP Registers - ISPF AH, ISPF AL, ISPF D and ISPC

ISP Flash Address-High Register (ISPF AH, \$F4)

	bit-7						bit-0	
Read:	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
Write:								
Reset value:	0	0	0	0	0	0	0	0

Note: FA15~FA8: Flash address-high for ISP function

ISP Flash Address-Low Register (ISPF AL, \$F5)

	bit-7						bit-0	
Read:	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
Write:								
Reset value:	0	0	0	0	0	0	0	0

Note: FA7~FA0: Flash address-low for ISP function

The ISPF AH & ISPF AL provides the 16-bit flash memory address for the ISP function. The Flash memory address should not include the ISP service program space address. If the flash memory address indicated by the ISPF AH & ISPF AL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

ISP Flash Data Register (ISPFDR, \$F6)

	bit-7						bit-0	
Read:	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Write:								
Reset value:	0	0	0	0	0	0	0	0

Note: FD7~FD0: Flash data for ISP function

The ISPFDR provides the 8-bit data for ISP function.

ISP Flash Control Register

	bit-7						bit-0	
Read:	START	Unused	Unused	Unused	Unused	Unused	F1	F0
Write:								
Reset value:	0	*	*	*	*	*	0	0

F[1:0] : ISP function select bit

START : ISP function start bit

= 1 : start ISP function which indicated by bit 1, bit 0 (F1, F0)

= 0 : no operation

The START bit is read-only by default, software must write three specific values 55H, AAH and 55H sequentially to the ISPFDR register to enable the START bit write attribute. That is:

```
MOV ISPFDR, #55H
```

```
MOV ISPFDR, #AAH
```

```
MOV ISPFDR, #55H
```

Any attempt to set START bit will not be allowed without the procedure above.

After START bit set to 1 then the VRS1000 hardware circuit will latch address and data bus and hold the program counter until the START bit reset to 0 when ISP function finished. User does not need to check the START bit status via software.

F[1:0]	ISP function
00	Byte program
01	Chip protect
10	Page erase
11	Chip erase

F[1:0] : ISP function select bit

One page of flash memory is 512 bytes.

To perform byte program/page erase ISP functions, the user must first specify the Flash address. When performing a page erase function, the VRS1000 will erase the entire Flash page that is pointed to by the address specified in the ISPFAR & ISPFAL registers. Example: flash address: \$XYMN

Page erase function will erase from \$XY00 to \$X(Y+1)FF (Y: even number)

Or page erase function will erase from \$X(Y-1)00 to \$XYFF (Y: odd number)

To perform the chip erase ISP function, the VRS1000 will erase all the flash program memory except the ISP service program space. Note that the VRS1000 will also un-protect the flash memory automatically.

Example: ISP service program for programming a byte - to program #22H into address 1005H

```
MOV SCONF,#04      ; enable VRS1000 ISP function
MOV ISPF AH,#10H   ; set flash address-high, 1 OH
MOV ISPF AL,#05H   ; set flash address-low, 05H
MOV ISPF D,#22H    ; set flash data to be programmed, data = 22H
MOV ISPC,#80H      ; start to program #22H to the flash address $1005H
                   ; after byte program is finished, START bit of ISPC will be reset to 0 automatically
                   ; program counter then points to the next instruction
```

ISP Registers - System Control Register (SCONF,\$BF)

	bit-7				bit-0			
Read:	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Write:								
Reset value:	0	*	*	*	*	0	1	0

The bit 2 (ISPE) of SCONF is ISP enable bit. User can enable overall VRS1000 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0.

The function of ISPE behaves like a security key. User can disable overall ISP function to prevent accidentally erasure.

Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generates a reset signal if the counter overflows. The WDT is useful for systems that are susceptible to noise, power glitches, or electronic discharge that can cause software dead loops or runaways. The WDT function allows user software a recovery mechanism from abnormal software conditions. The WDT is different from Timer0, Timer1 and Timer2 of the standard 80C52. To prevent a WDT from resetting the MCU, software must periodically clear the WDT counter. The user should check the WDR bit of SCONF register whenever an unpredicted reset has taken place.

The WDT has a selectable divider input for the time base source clock. To select the divider input, bit2-bit0 (PS2~PS0) of the Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enabling the WDT, set bit 7 (WDTE) of the WDTC to 1. Once WDTE set to 1, the 16-bit counter will start to count with the selected time base source clock configured in PS2~PS0. It will generate a reset signal if an overflow takes place. The WDTE bit will be cleared to 0 automatically when VRS1000 has been reset by either a hardware or WDT reset.

Clearing the WDT is done by setting CLEAR bit of the WDTC to 1. This will clear the contents of the 16-bit counter and restart the counter.

Watch Dog Timer Registers: WDTC and SCONF

	bit-7					bit-0		
Read:	WDTE	Unused	CLEAR	Unused	Unused	PS2	PS1	PS0
Write:								
Reset value:	0	*	0	*	*	0	0	0

WDTE: Watch Dog Timer enable bit

CLEAR: Watch Dog Timer counter clear bit

PS[2:0]: clock source divider bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHZ
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

Watch Dog Timer Register - System Control Register (SCONF, \$BF)

	bit-7					bit-0		
Read:	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Write:								
Reset value:	0	*	*	*	*	0	1	0

Bit 7 (WDR) of SCONF is the Watch Dog Timer Reset bit. It will be set to 1 when a reset signal is generated by the WDT overflow. The user should check WDR bit whenever an unpredicted reset has taken place.

Reduce EMI Function

The VRS1000 can be set up to reduce its EMI (electro-magnetic interference) by setting bit 0 (ALEI) of the SCONF register to a 1. This function will inhibit the in Fosc/6Hz clock signal output to the ALE pin.

Specific Pulse Width Modulation (SPWM)

The Specific Pulse Width Modulation (SPWM) module has five 8-bit channels. Each channel uses an 8-bit SPWM data register (SPWMD) to set the number of continuous pulses within a SPWM frame cycle.

SPWM Function Description:

Each 8-bit SPWM channel is composed of an 8-bit register consists of a 5-bit SPWM (5 MSBs) and a 3-bit (LSBs) binary rate multiplier (BRM). The 5-bit SPWM determines the pulse length of the output. The 3-bit BRM generates and inserts narrow pulses among the 8-SPWM-cycle frame.

The number of pulses generated is equal to the number programmed in the 3-bit BRM. The BRM is used to generate an equivalent 8-bit resolution SPWM type DAC with a reasonably high repetition rate through a 5-bit SPWM clock speed. The PDIV[1:0] settings of the SPWMC (\$A3) register is used to derive the SPWM clock from Fosc ($F_{osc}/2^{(PDIV[1:0]+1)}$).

The SPWM output cycle frame repetition rate (frequency) equals (SPWM clock)/32 which is $[F_{osc}/2^{(PDIV[1:0]+1)}]/32$.

SPWM Registers - P1 CON, SPWMC, SPWMR[4:0]

SPWM Registers - Port1 Configuration Register (P1 CON, \$9B)

	bit-7					bit-0		
Read:	SPWM4E	SPWM3E	SPWM2E	SPWM1E	SPWM0E	Unused	Unused	Unused
Write:								
Reset value:	0	0	0	0	0	*	*	*

SPWM[4:0]E : When bit is set to one, the corresponding SPWM pin is active as a SPWM function. When the bit is cleared, the corresponding SPWM pin is active as an I/O pin. These five bits are cleared upon reset.

SPWM Registers - SPWM Control Register (SPWMC, \$A3)

	bit-7						bit-0	
Read:	Unused	Unused	Unused	Unused	Unused	Unused	PDIV1	PDIV0
Write:								
Reset value:	*	*	*	*	*	*	0	0

PDIV[1:0] : These two bits form a frequency divider for the input clock.

PDIV1	PDIV0	Divider	SPWM clock, Fosc=20MHz	SPWM clock, Fosc=24MHz
0	0	2	10MHz	12MHz
0	1	4	5MHz	6MHz
1	0	8	2.5MHz	3MHz
1	1	16	1.25MHz	1.5MHz

SPWM Data Register (SPWMD[4:0], \$AC, \$A4~\$A7)

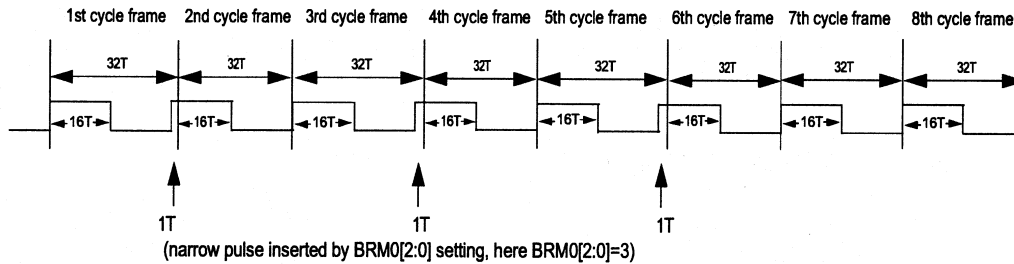
	bit-7					bit-0		
Read:	SPWMD [4:0]4	SPWMD [4:0]3	SPWMD [4:0]2	SPWMD [4:0]1	SPWMD [4:0]0	BRM [4:0]2	BRM [4:0]1	BRM [4:0]0
Write:								
Reset value:	0	0	0	0	0	0	0	0

SPWMD[4:0][4:0] : content of SPWM Data Register. It determines duty cycle of SPWM output waveform.
BRM[4:0][2:0] : will insert narrow pulses among an B-SPWM-cycle frame.

N = BRM[4:0][2:0]	Number of SPWM cycles inserted in an 8-cycle frame
XX1	1
X1X	2
1XX	3

Example of SPWM Timing Diagram

```
MOV SPWMD0 #83H      ; SPWMD04:0]=10h (=16T high, 16T low), BRM02:0] = 3
MOV P1CON, #08H     ; Enable P1.3 as PWM output pin
```



SPWM clock = $1 / T = F_{osc} / 2^{(PDIV+1)}$
The SPWM output cycle frame frequency = SPWM clock / 32 = $[F_{osc} / 2^{(PDIV+1)}] / 32$

If $F_{osc}=20\text{MHz}$, $PDIV[1:0]$ of SPWWC=#03H, then SPWM clock = $20\text{MHz} / 2^4 = 20\text{MHz} / 16 = 1.25\text{MHz}$. PWM output cycle frame frequency = $(20\text{MHz} / 2^4) / 32 = 39.1 \text{ KHz}$.

Operating Conditions

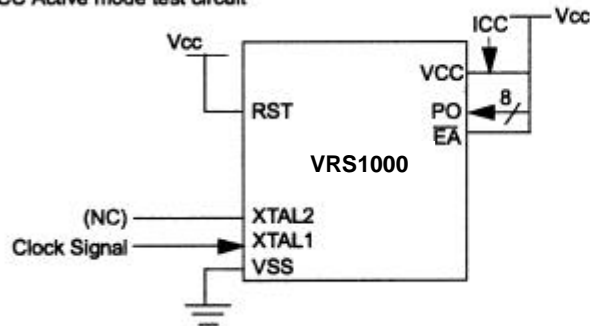
Symbol	Description	Min.	Typ.	Max.	Unit	Remarks
TA	Operating temperature	0	25	70	°C	Ambient temperature under bias
TS	Storage temperature	-55	25	155	°C	
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 16	Oscillator Frequency	3.0	16	16	MHz	For 5V application
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

DC Characteristics

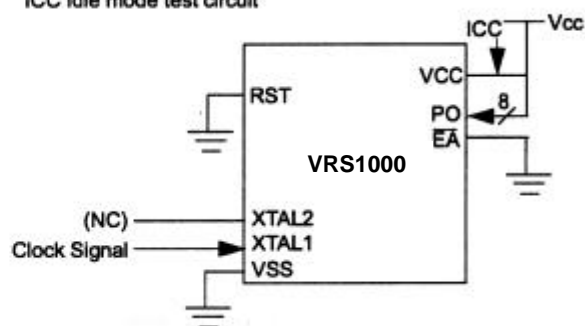
(16/25/40 MHz, typical operating conditions, valid for VRS1000 series)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	Port 0, 1, 2, 3, 4, #EA	-0.5	1.0	V	VCC = 5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	VCC = 5V
VIH1	Input High Voltage	Port 0, 1, 2, 3, 4, #EA	2.0	VCC+0.5	V	VCC = 5V
VIH2	Input High Voltage	RES, XTAL1	70% VCC	VCC+0.5	V	VCC = 5V
VOL1	Output Low Voltage	Port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	Port 1, 2, 3, 4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	Port 0	2.4		V	IOH=-800uA
			90%VCC		V	IOH=-80uA
VOH2	Output High Voltage	Port 1, 2, 3, 4, ALE, #PSEN	2.4		V	IOH=-60uA
			90% VCC		V	IOH=-10uA
IIL	Logical 0 Input Current	Port 1, 2, 3, 4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	Port 1, 2, 3, 4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	Port 0, #EA		±10	uA	0.45V < Vin < VCC
R RES	Reset Pulldown Resistance	RES	50	300	Kohm	
C ₁₀	Pin Capacitance			10	pF	Fre = 1 MHz, Ta=25°C
ICC	Power Supply Current	VDD		20	mA	Active mode, 40MHz
				15	mA	Active mode 25MHz
				10	mA	Active mode 16MHz
				10	mA	Idle mode, 40MHz
				7.5	mA	Idle mode 25MHz
				6	mA	Idle mode, 16MHz
				150	uA	Power down mode

ICC Active mode test circuit



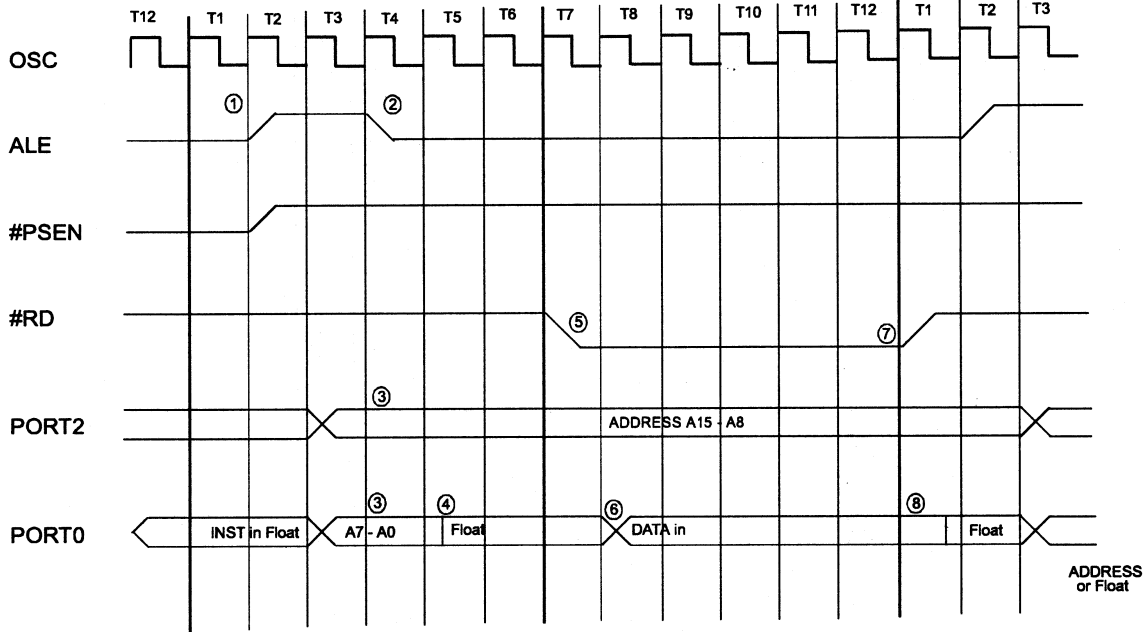
ICC Idle mode test circuit



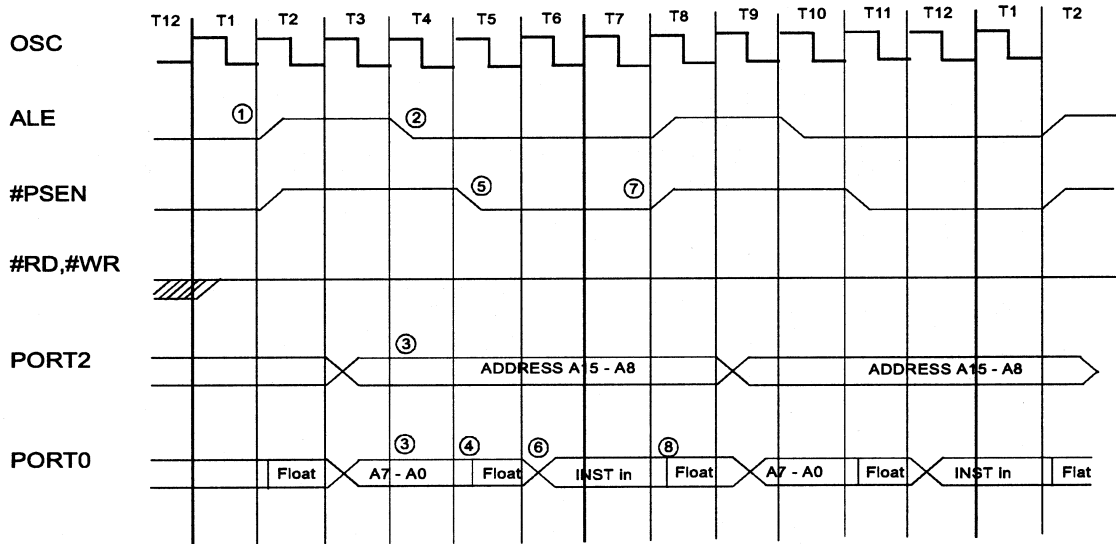
AC Characteristics

Symbol	Parameter	Valid Cycle	f osc 16			Variable f osc			Unit
			Min.	Type	Max.	Min.	Type	Max.	
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS
T AVI V	Address to Valid Instruction In	RD			292			5xT - 20	nS
T PLAZ	#PSEN low to Address Float	RD			10			10	nS
T LLRH	#RD pulse width	RD	365			6xT - 10			nS
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS
T RHDX	Data Hold after #RD	RD	0			0			nS
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS
T QVWH	Data Valid to #WR high	WRT	403			7xT - 35			nS
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS
T WHQX	Data hold after #WR	WRT	73			T + 10			nS
T RLAZ	#RD low to Address Float	RD						5	nS
T YALH	#W R or #RD high to ALE high	RD/WRT	53		72	T - 10		T+10	nS
T CHCL	Clock fall time								nS
T CLCX	Clock low time								nS
T CLCH	Clock rise time								nS
T CHCX	Clock high time								nS
T, TCLCL	Clock period		63				1/fosc		nS

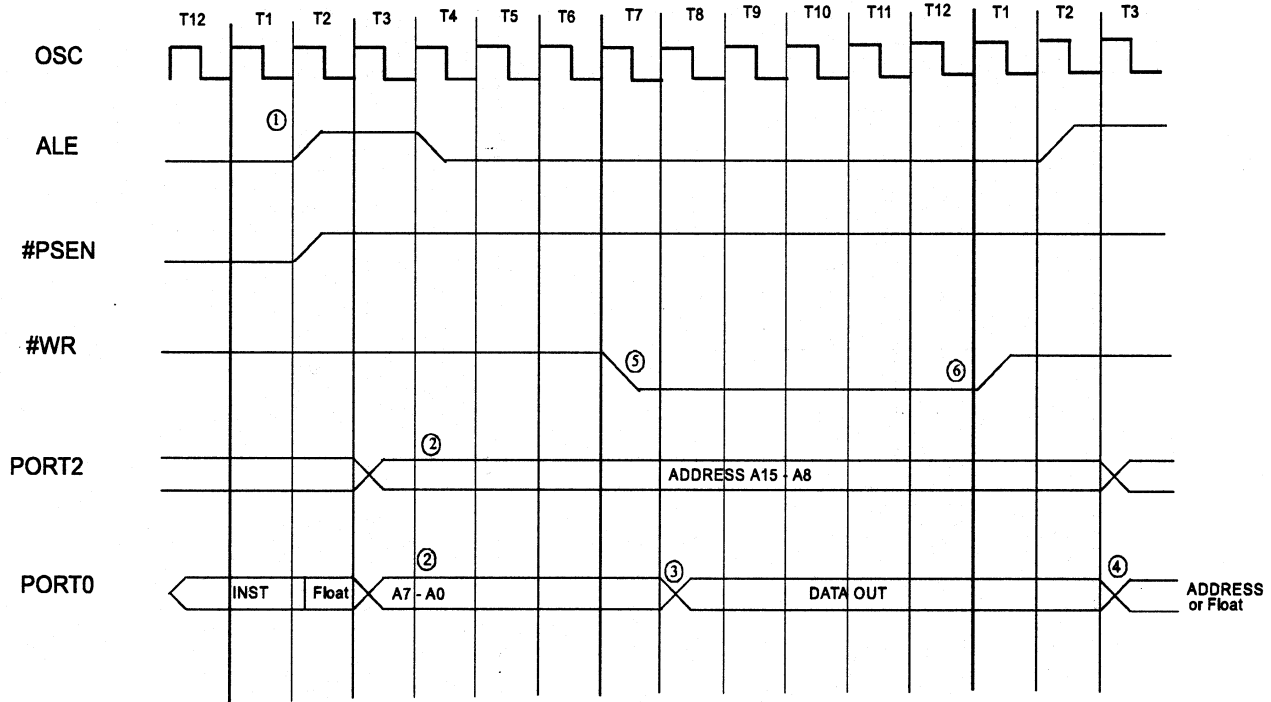
Data Memory Read Cycle Timing



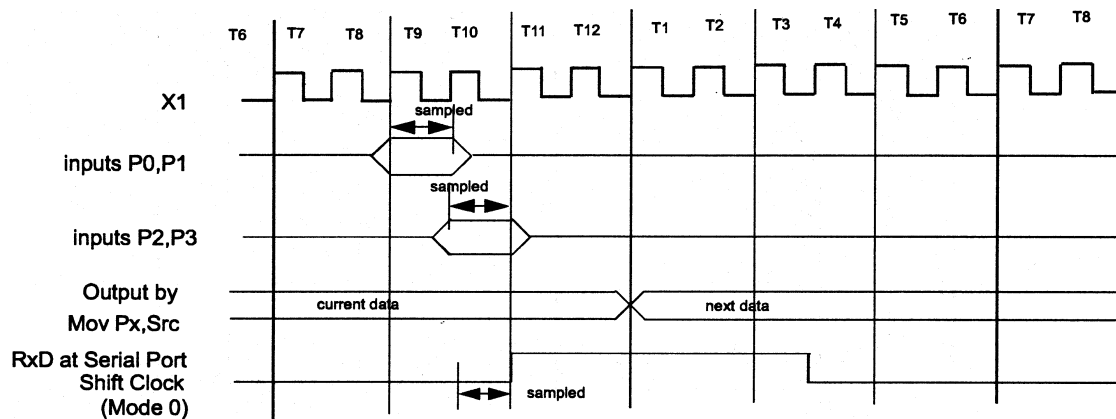
Program Memory Read Cycle Timing



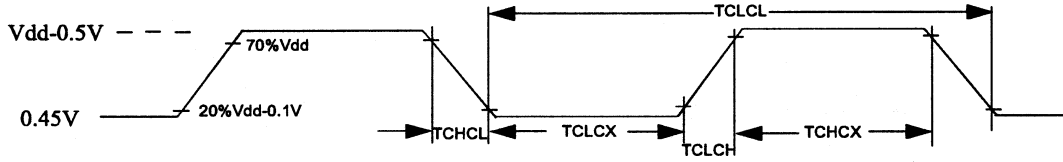
Data Memory Write Cycle Timing



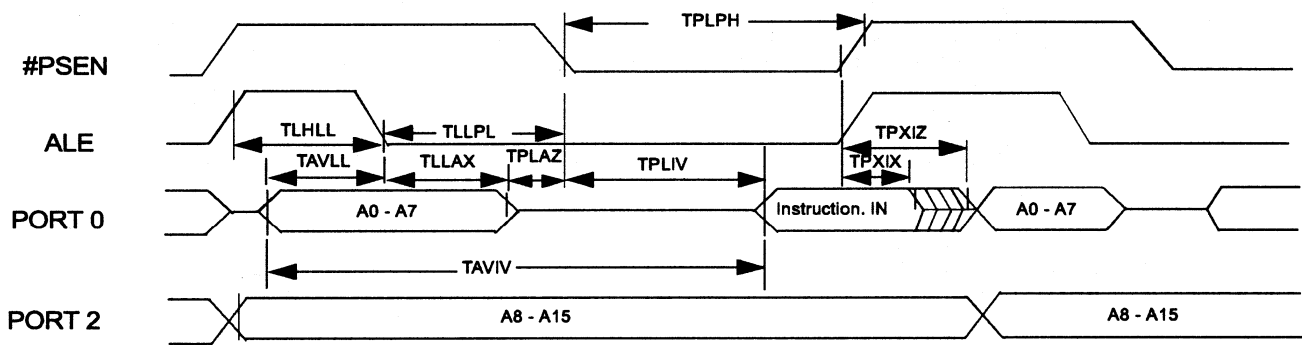
I/O Ports Timing



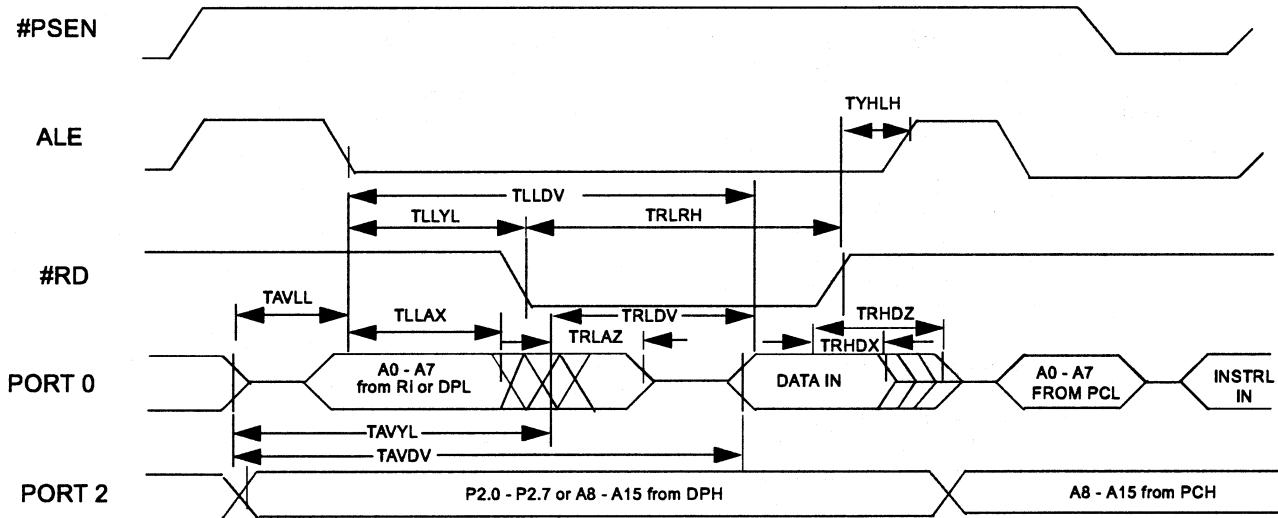
Timing Critical Requirement of External Clock (VSS=0.0v is assumed)



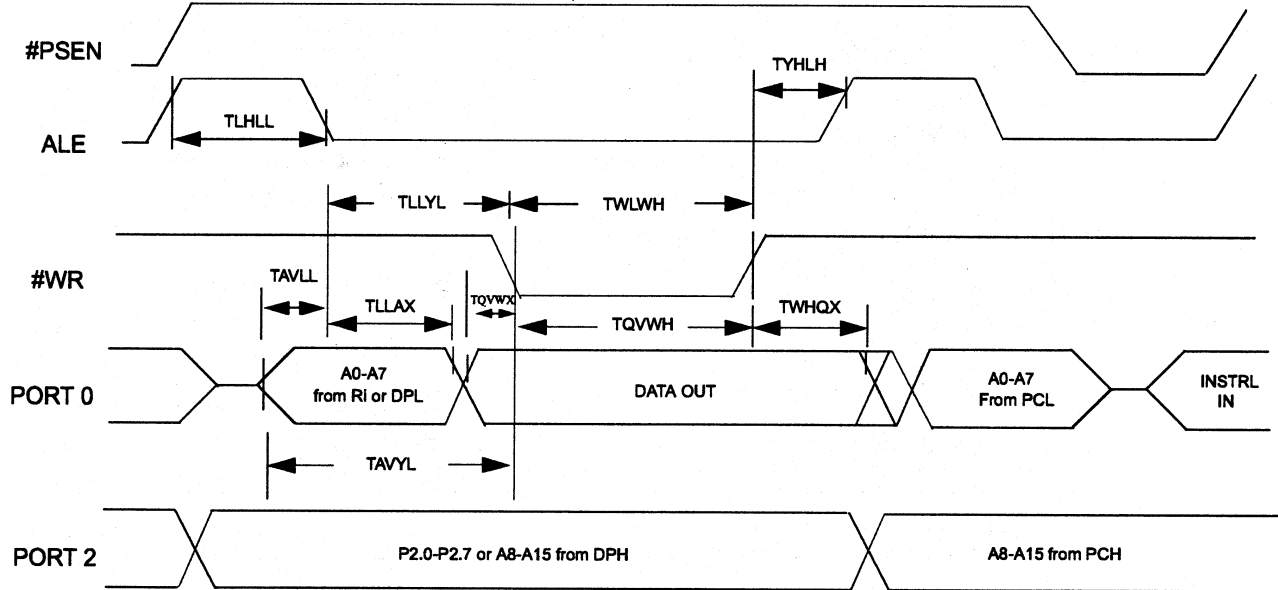
External Program Memory Read Cycle



External Data Memory Read Cycle



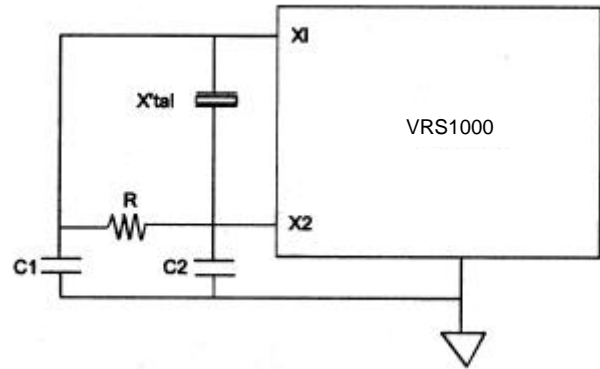
External Data Memory Write Cycle



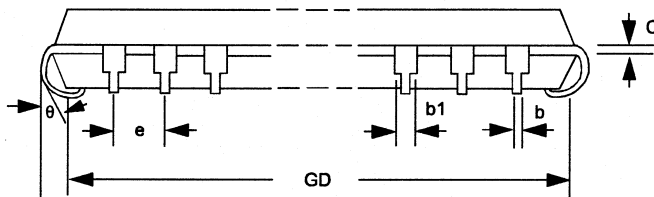
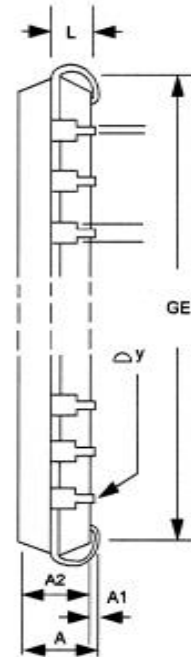
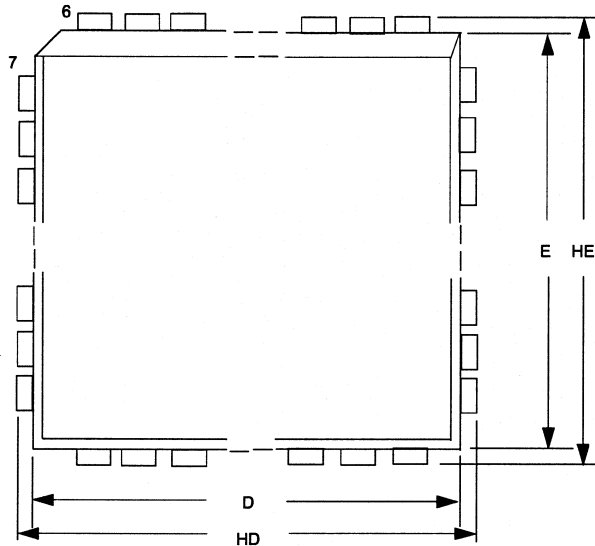
Application Reference

Valid for VRS1000				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 p	30 p	30 p	30 p
C2	30 p	30 p	30 p	30 p
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	10 pF	2 pF
C2	30 pF	15 pF	10 pF	2 pF
R	open	62KO	6.8KO	4.7KO

Note: Oscillator circuit performance may differ with different crystal or ceramic resonators in higher oscillation frequency. This is due to specific crystal or ceramic resonator characteristics. User should check with the crystal or ceramic resonator manufacturer for the appropriate values for the external components.



44 Plastic Chip Carrier (PLCC)

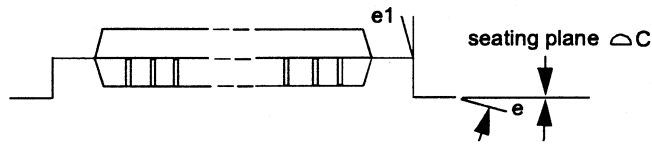
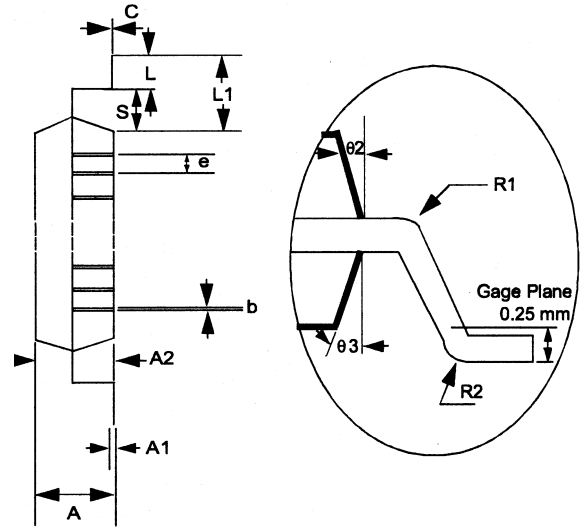
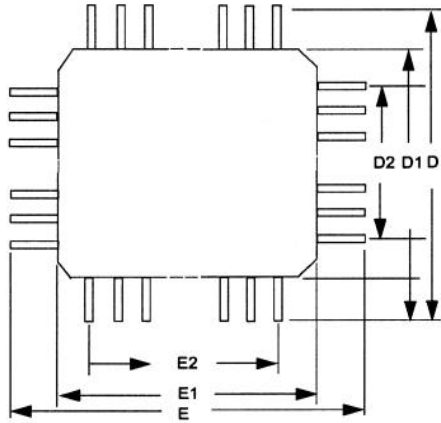


Note:

1. Dimensions D & E do not include interlead Flash.
2. Dimension B1 does not include dambar protrusion/intrusion.
3. Controlling dimension: inch
4. General appearance spec should be based on final visual inspection spec.

Symbol	Dimension in inch	Dimension in mm
	Minimal/Maximal	Minimal/Maximal
A	-/0.185	-/4.70
A1	0.020/-	0.51/
A2	0.145/0.155	3.68/3.94
b1	0.026/0.032	0.66/0.81
b	0.016/0.022	0.41/0.56
C	0.008/0.014	0.20/0.36
D	0.648/0.658	16.46/16.71
E	0.648/0.658	16.46/16.71
e	0.050 BSC	1.27 BSC
GD	0.590/0.630	14.99/16.00
GE	0.590/0.630	14.99/16.00
HD	0.680/0.700	17.27/17.78
HE	0.680/0.700	17.27/17.78
L	0.090/0.110	2.29/2.79
?	-/0.004	-/0.10
Δy	/	/

40 Plastic Quad Flat Package



Note:

1. Dimension D1 and E1 do not include mold protrusion.
2. Allowance protrusion is 0.25mm per side.
3. Dimensions D1 and E1 do not include mold mismatch and are determined datum plane.
4. Dimension b does not include dambar protrusion.
5. Allowance dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the lead foot.

Symbol	Dimension in inch	Dimension in mm
	Minimal/Maximal	Minimal/Maximal
A	-/0.100	-/2.55
Al	0.006/0.014	0.15/0.35
A2	0.071 / 0.087	1.80/2.20
b	0.012/0.018	0.30/0.45
c	0.004 / 0.009	0.09/0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73/1.03
L1	0.063	1.60
R1	0.005/-	0.13/-
R2	0.005/0.012	0.13/0.30
S	0.008/-	0.20/-
0	0°/7°	as left
? 1	0°/-	as left
? 2	10° REF	as left
? 3	7° REF	as left
△ C	0.004	0.10

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