



## CMOS Micro-Power Comparator plus Voltage Follower

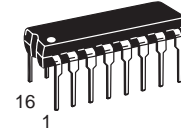
The MC14578 is an analog building block consisting of a very-high input impedance comparator. The voltage follower allows monitoring the noninverting input of the comparator without loading.

Four enhancement-mode MOSFETs are also included on chip. These FETs can be externally configured as open-drain or totem-pole outputs. The drains have on-chip static-protecting diodes. Therefore, the output voltage must be maintained between  $V_{SS}$  and  $V_{DD}$ .

The chip requires one external component. A  $3.9\text{ M}\Omega \pm 10\%$  resistor must be connected from the  $R_{bias}$  pin to  $V_{DD}$ . This circuit is designed to operate in smoke detector systems that comply with UL217 and UL268 specifications.

- Applications:
  - Pulse Shapers
  - Line-Powered Smoke Detectors
  - Threshold Detectors
  - Liquid/Moisture Sensors
  - Low-Battery Detectors
  - CO Detector and Micro Interface
- Operating Voltage Range: 3.5 to 14 V
- Operating Temperature Range:  $-30^\circ$  to  $70^\circ\text{C}$
- Input Current (IN + Pin):  $\pm 1\text{ pA}$  @  $25^\circ\text{C}$  (DIP Only)
- Quiescent Current:  $10\text{ }\mu\text{A}$  @  $25^\circ\text{C}$
- Electrostatic Discharge (ESD) Protection Circuitry on All Pins

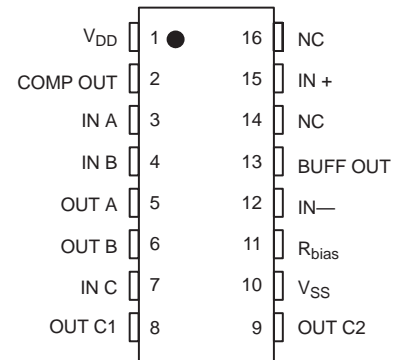
# MC14578



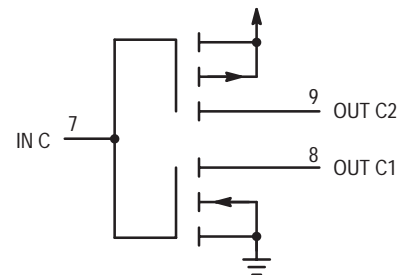
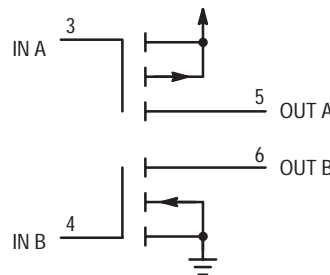
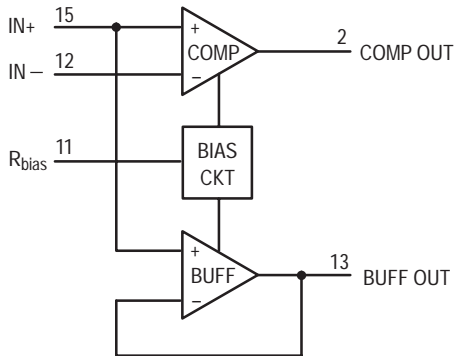
**P SUFFIX  
PLASTIC DIP  
CASE 648-08**

**ORDERING INFORMATION  
MC14578P PLASTIC DIP**

### PIN ASSIGNMENT



### LOGIC DETAIL



PIN 1 =  $V_{DD}$   
PIN 10 =  $V_{SS}$   
PINS 14, 16 = NO CONNECTION



**MAXIMUM RATINGS\*** (Voltages Referenced to  $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to +14	V
$V_{in}$	DC Input Voltage	- 0.5 to $V_{DD} + 0.5$	V
$V_{out}$	DC Output Voltage	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}$	DC Input Current, Except IN +	$\pm 10$	mA
$I_{in}$	DC Input Current, IN +	$\pm 1.0$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{DD}$	DC Supply Current, $V_{DD}$ and $V_{SS}$ Pins	$\pm 50$	mA
$P_D$	Power Dissipation, per Package	500	mW
$T_{stg}$	Storage Temperature	- 65 to +150	°C
$T_L$	Lead Temperature (10-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

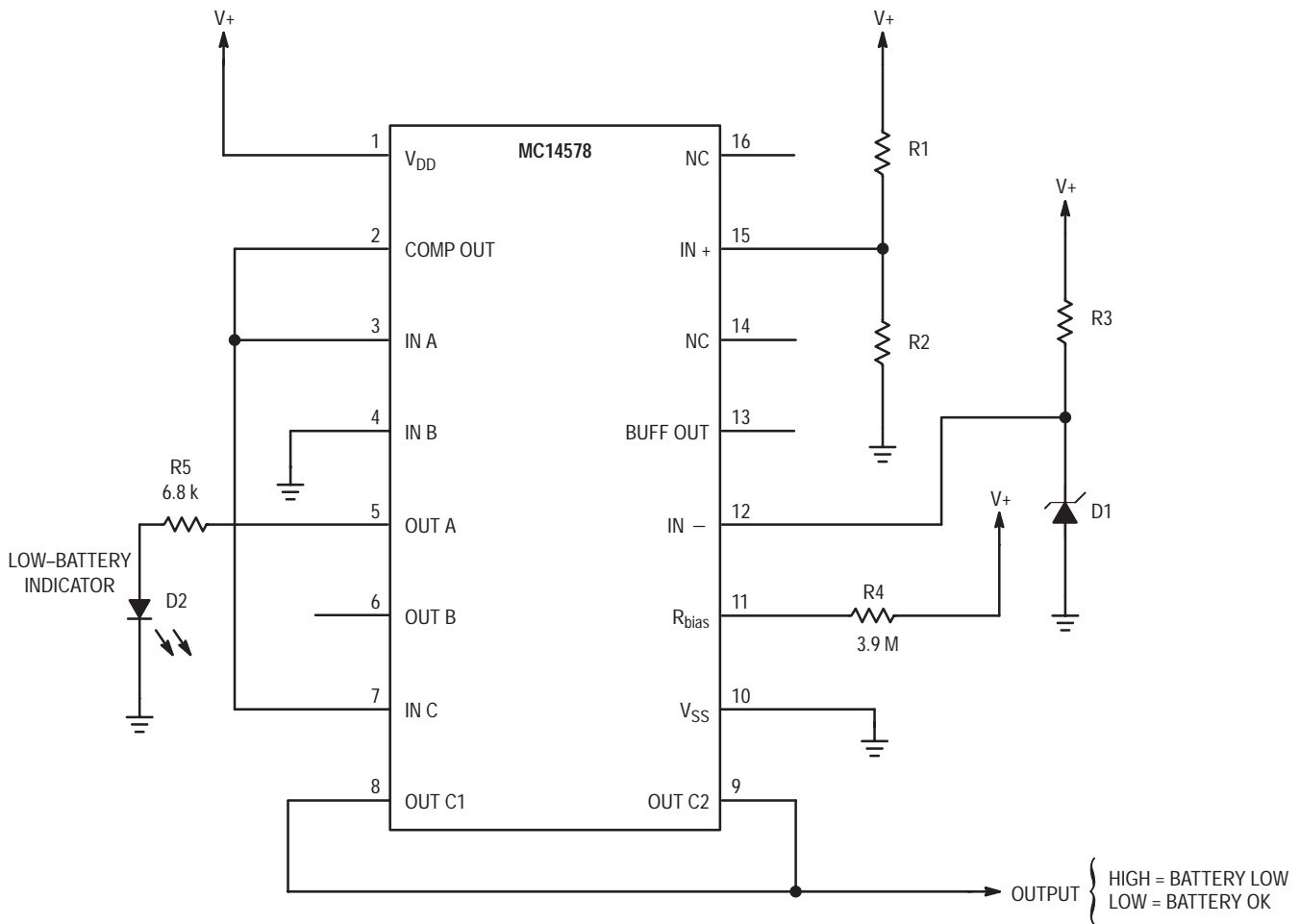
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ ,  $R_{bias} = 3.9\text{ M}\Omega$  to  $V_{DD}$ ,  $T_A = -30^\circ$  to  $70^\circ\text{C}$  Unless Otherwise Indicated)

Symbol	Parameter	Test Condition	$V_{DD}$ V	Guaranteed Limit	Unit
$V_{DD}$	Power Supply Voltage Range		—	3.5 to 14.0	V
$V_{IL}$	Maximum Low-Level Input Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2.	$V_{out} = 9.0\text{ V}$ , $ I_{out}  < 1\ \mu\text{A}$	10.0	2.0	V
$V_{IH}$	Minimum High-Level Input Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2.	$V_{out} = 1.0\text{ V}$ , $ I_{out}  < 1\ \mu\text{A}$	10.0	8.0	V
$V_{IO}$	Comparator Input Offset Voltage	$T_A = 25^\circ\text{C}$ , Over Common Mode Range	10.0	$\pm 50$	mV
		$T_A = 0^\circ$ to $50^\circ\text{C}$ , Over Common Mode Range	3.5 to 14.0	$\pm 75$	
$V_{CM}$	Comparator Common Mode Voltage Range		3.5 to 14.0	0.7 to $V_{DD} - 1.5$	V
$V_{OL}$	Maximum Low-Level Comparator Output Voltage	IN +: $V_{in} = V_{SS}$ , IN -: $V_{in} = V_{DD}$ , $I_{out} = 30\ \mu\text{A}$	10.0	0.5	V
$V_{OH}$	Minimum High-Level Comparator Output Voltage	IN +: $V_{in} = V_{DD}$ , IN -: $V_{in} = V_{SS}$ , $I_{out} = -30\ \mu\text{A}$	10.0	9.5	V
$V_{OO}$	Buffer Amp Output Offset Voltage	$R_{load} = 10\text{ M}\Omega$ to $V_{DD}$ or $V_{SS}$ , Over Common Mode Range	—	$\pm 100$	mV
$V_{OL}$	Maximum Low-Level Output Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2.	OUT C1, OUT C2: $I_{out} = 1.1\text{ mA}$	10.0	0.5	V
		OUT A, OUT B: $I_{out} = 270\ \mu\text{A}$	10.0	0.5	V
$V_{OH}$	Minimum High-Level Output Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2.	OUT C1, OUT C2: $I_{out} = -1.1\text{ mA}$	10.0	9.5	V
		OUT A, OUT B: $I_{out} = 270\ \mu\text{A}$	10.0	9.5	V
$I_{in}$	Maximum Input Leakage Current IN + (DIP Only) IN + (DIP Only) IN + (SOG), IN A, IN B, IN C, IN -	$T_A = 25^\circ\text{C}$ , 40% R.H., $V_{in} = V_{SS}$ or $V_{DD}$	10.0	$\pm 1.0$	pA
		$T_A = 50^\circ\text{C}$ , $V_{in} = V_{SS}$ or $V_{DD}$	10.0	$\pm 6.0$	
		$V_{in} = V_{SS}$ or $V_{DD}$	10.0	$\pm 40$	nA
$I_{OZ}$	Maximum Off-State MOSFET Leakage Current	IN A, IN C: $V_{in} = V_{DD}$ , OUT A, OUT C2: $V_{out} = V_{SS}$ or $V_{DD}$	10.0	$\pm 100$	nA
		IN B, IN C: $V_{in} = V_{SS}$ , OUT B, OUT C1: $V_{out} = V_{SS}$ or $V_{DD}$	10.0	$\pm 100$	
$I_{DD}$	Maximum Quiescent Current	$T_A = 25^\circ\text{C}$ IN A, IN B, IN C: $V_{in} = V_{SS}$ or $V_{DD}$ , $ V_{IN+} - V_{IN-}  = 100\text{ mV}$ , $I_{out} = 0\ \mu\text{A}$	10.0	10	$\mu\text{A}$
$C_{in}$	Maximum Input Capacitance IN + Other Inputs	$f = 1\text{ kHz}$	—	5.0	pF
			—	15	

APPLICATIONS INFORMATION



NOTE: IN + and IN - have very high input impedance. Interconnect to these pins should be as short as possible.

Figure 1. Low-Battery Detector

EXAMPLE VALUES

Near the switchpoint, the comparator output in the circuit of Figure 1 may chatter or oscillate. This oscillation appears on the signal labelled OUTPUT. In some cases, the oscillation in the transition region will not cause problems. For example, an MPU reading OUTPUT could sample the signal two or three times to ensure a solid level is attained. But, in a low battery detector, this probably is not necessary.

To eliminate comparator chatter, hysteresis can be added as shown in Figure 2. The circuit of Figure 2 requires slightly more operating current than the Figure 1 arrangement.

R1	R2	R3	Nominal Trip Point
470 kΩ	1.3 MΩ	20 kΩ	4.08 V
820 kΩ	1.2 MΩ	39 kΩ	5.05 V
1.2 MΩ	1.2 MΩ	62 kΩ	6.00 V

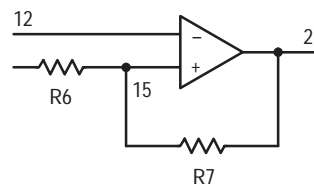
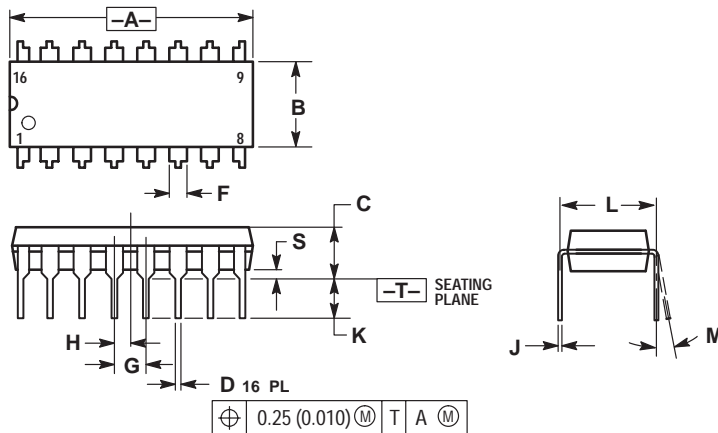


Figure 2. Adding Hysteresis

**PACKAGE DIMENSIONS**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01


- STYLE 1:
- |        |         |
|--------|---------|
| PIN 1. | CATHODE |
| 2.     | CATHODE |
| 3.     | CATHODE |
| 4.     | CATHODE |
| 5.     | CATHODE |
| 6.     | CATHODE |
| 7.     | CATHODE |
| 8.     | CATHODE |
| 9.     | ANODE   |
| 10.    | ANODE   |
| 11.    | ANODE   |
| 12.    | ANODE   |
| 13.    | ANODE   |
| 14.    | ANODE   |
| 15.    | ANODE   |
| 16.    | ANODE   |
- STYLE 2:
- |        |              |
|--------|--------------|
| PIN 1. | COMMON DRAIN |
| 2.     | COMMON DRAIN |
| 3.     | COMMON DRAIN |
| 4.     | COMMON DRAIN |
| 5.     | COMMON DRAIN |
| 6.     | COMMON DRAIN |
| 7.     | COMMON DRAIN |
| 8.     | COMMON DRAIN |
| 9.     | GATE         |
| 10.    | SOURCE       |
| 11.    | GATE         |
| 12.    | SOURCE       |
| 13.    | GATE         |
| 14.    | SOURCE       |
| 15.    | GATE         |
| 16.    | SOURCE       |

**CASE 648-08  
ISSUE R**

# NOTES

# NOTES

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